WHAT IS CLAIMED IS:

1. A tri-state detection circuit, comprising:

a first input port for receiving a tri-state input signal;

a clock input port for receiving a clocking signal;

a first output port;

a second output port coupled to said first input port;

a D-flip-flop having a D input, a clock input CLK, and a Q output, said D input being tied high, said clock input CLK being coupled to said first input port, and said Q output being coupled to said first output port; and

a buffer having a buffer input and a buffer output, said buffer input being coupled to said clock input port, and said buffer output being coupled to said clock input CLK of said D-flip-flop.

2. The tri-state detection circuit of claim 1, wherein said buffer is able to sink or source about 0.1 milliamps of current.

3. The tri-state detection circuit of claim 1, wherein when said first input port is at a logic low level, said clock input CLK of said D-flip-flop will not detect an edge transition of said clocking signal supplied to said clock input port.

4. The tri-state detection circuit of claim 3, wherein said logic low level at said first input port is supplied to said second output port.

5. The tri-state detection circuit of claim 1, wherein when said first input port is at a logic high level, said clock input CLK of said D-flip-flop will not detect an edge transition of said clocking signal supplied to said clock input port.

6. The tri-state detection circuit of claim 5, wherein said logic high level at said first input port is supplied to said second output port.

7. The tri-state detection circuit of claim 1, wherein said first input port, said second output port, said clock input CLK and said buffer output are connected to a common node.

8. The tri-state detection circuit of claim 1, further comprising a clock source for supplying said clocking signal to said clock input port.

9. The tri-state detection circuit of claim 1, wherein said tri-state input signal is supplied by a tri-state input device.

10. The tri-state detection circuit of claim 1, wherein said first output port and said second output port are configured to be connected to a decoding circuit that provides three discrete outputs corresponding, respectively, to a floating level, a logic high level and a logic low level present at said first input port.

11. An electronic apparatus having a tri-state detection circuit used in facilitating communications with another electronic apparatus, said tri-state detection circuit comprising:

a first input port;

a clock input port;

a first output port;

a second output port;

a D-flip-flop, said D-flip-flop having a D input, a clock input CLK, and a Q output, said D input being tied high, said clock input CLK being connected to said first input port, and said Q output being connected to said first output port; and

a buffer having a buffer input and a buffer output, said buffer input being connected to said clock input port, said buffer output being connected to said clock input CLK of said D-flip-flop, said buffer output being connected to said first input port, and said buffer output being connected to said second output port.

12. The electronic apparatus of claim 11, wherein said buffer is able to sink or source about 0.1 milliamps of current.

13. The electronic apparatus of claim 11, wherein when said first input port is at a logic low level, said clock input CLK of said D-flip-flop will not detect an edge transition of a clocking signal supplied to said clock input port.

14. The electronic apparatus of claim 13, wherein said logic low level at said first input port is supplied to said second output port.

15. The electronic apparatus of claim 11, wherein when said first input port is at a logic high level, said clock input CLK of said D-flip-flop will not detect an edge transition of a clocking signal supplied to said clock input port.

16. The electronic apparatus of claim 15, wherein said logic high level at said first input port is supplied to said second output port.

17. The electronic apparatus of claim 11, wherein said first input port is connected to said second output port.

18. The electronic apparatus of claim 11, further comprising a clock source for supplying a clocking signal to said clock input port.

19. The electronic apparatus of claim 11, wherein said first input port is connected to a tri-state input device.

20. The electronic apparatus of claim 11, wherein said first output port and said second output port are configured to be connected to a decoding circuit that provides three discrete outputs corresponding, respectfully, to a floating level, a logic high level and a logic low level present at said first input port.

21. The electronic apparatus of claim 11, wherein said electronic apparatus is one of a supply item and an imaging apparatus.

22. The electronic apparatus of claim 21, wherein said supply item is an ink jet printhead cartridge.

23. The electronic apparatus of claim 21, wherein said imaging apparatus is an ink jet printer.

24. A supply item comprising a circuit including a tri-state input port, and said supply item having at least three modes of operation, wherein a particular mode of operation of said at least three modes of operation is selected based on a signal level of a tri-state input signal supplied to said tri-state input port.

25. The supply item of claim 24, wherein said circuit further includes:

a clock input port for receiving a clocking signal;

a first output port;

a second output port coupled to said tri-state input port;

a D-flip-flop having a D input, a clock input CLK, and a Q output, said D input being tied high, said clock input CLK being coupled to said tri-state input port, and said Q output being coupled to said first output port; and

a buffer having a buffer input and a buffer output, said buffer input being coupled to said clock input port, and said buffer output being coupled to said clock input CLK of said D-flip-flop.

26. The supply item of claim 25, further comprising a decoding circuit coupled to said first output port and said second output port, said decoding circuit providing three discrete outputs corresponding, respectively, to a floating level, a logic high level and a logic low level present at said tri-state input port.

27. The supply item of claim 26, wherein each of said three discrete outputs is respectively coupled to one of at least three selectable mode devices.

28. The supply item of claim 24, wherein said supply item is a printhead cartridge.

29. The supply item of claim 24, wherein said circuit is formed on a printhead attached to said supply item.

30. An imaging apparatus, comprising:

a controller; and

a supply item including a circuit having a tri-state input port coupled to said controller, said supply item having at least three modes of operation, wherein a particular mode of operation of said at least three modes of operation is selected based on a signal level of a tri-state input signal supplied to said tri-state input port by said controller.

31. The imaging apparatus of claim 30, wherein said circuit further includes:

a clock input port for receiving a clocking signal;

a first output port;

a second output port coupled to said tri-state input port;

a D-flip-flop having a D input, a clock input CLK, and a Q output, said D input being tied high, said clock input CLK being coupled to said tri-state input port, and said Q output being coupled to said first output port; and

a buffer having a buffer input and a buffer output, said buffer input being coupled to said clock input port, and said buffer output being coupled to said clock input CLK of said D-flip-flop.

32. The imaging apparatus of claim 31, further comprising a decoding circuit coupled to said first output port and said second output port, said decoding circuit providing three discrete outputs corresponding, respectively, to a floating level, a logic high level and a logic low level present at said tri-state input port.

33. The imaging apparatus of claim 32, wherein each of said three discrete outputs is respectively coupled to one of at least three selectable mode devices.

34. The imaging apparatus of claim 30, wherein said supply item is a printhead cartridge.

35. The imaging apparatus of claim 30, wherein said circuit is formed on a printhead attached to said supply item.